ABSTRACT OF THE DISCLOSURE

[0028] Semiconductor wafer tray positioning, such as can be used in rapid thermal processing (RTP), rapid thermal annealing (RTA), and other semiconductor fabrication processes, is disclosed. A housing, such as a quartz tube, to receive a wafer tray includes at least four positioning kits. Each positioning kit includes a primary outside edge and an inside edge. The primary outside edge at least substantially corresponds to an interior sidewall of the housing. The inside edge is opposite of the primary outside edge, and has a groove that at least substantially corresponds to a part of a frame of the wafer tray. The groove is receptive to the part of the frame of the wafer tray, to assist maintaining the wafer tray in a stable position when the tray is completely positioned in the housing.